AMENDMENTS TO THE CLAIMS

Please replace all prior versions of the claims with the following claim listing:

Claims:

1. (Previously Presented) A circuit for detecting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a clock generating circuit configured to generate a master clock signal, a DCE clocking signal, and an internal clocking signal, each of the DCE clocking signal and internal clocking signal having a first frequency that is a fraction of the frequency of the master clock signal;

a sample enable generator configured to receive the master clock signal and the internal clocking signal and to generate a first sample enable signal at a first time and a second sample enable signal at a second time, the second time being subsequent to the first time; and

a sample comparator having inputs that receive said first sample enable signal, said second enable signal and said DTE data signal, the sample comparator configured to sample the DTE data signal at the first time and sample the DTE data signal at the second time, the sample comparator further configured to compare the DTE data signal sampled at the first time with the DTE data signal sampled at the second time and determine, from the comparison, whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

2. (Original) The circuit of claim 1, wherein the frequency of said master clocking signal is approximately 8 times the frequency of said DCE clocking signal.

3. (Original) The circuit of claim 1, wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal.

4. (Previously Presented) The circuit of claim 1, wherein said sample comparator generates a selector control signal when the sample comparator determines that the DTE data signal has undergone a transition.

5. (Previously Presented) The circuit of claim 4, wherein the clock generating circuit comprises:

a clock generator that generates the DCE clocking signal;

an inverter that produces an inverted DCE clocking signal from the DCE clocking signal; and

a selector that receives the DCE clocking signal and the inverted DCE clocking signal and produces the internal clocking signal that is selected, in response to the selector control signal, from the group consisting of the DCE clocking signal and the inverted DCE clocking signal.

13 ~~6.~~ (Previously Presented) A circuit for detecting and correcting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal;

means for deriving a DCE clocking signal and an internal clocking signal from said master clock signal, said internal clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal;

means for comparing said first sample to said second sample;

means for generating a selector control signal if said first sample is different from said second sample;

means for inverting said internal clocking signal to produce an inverted clocking signal; and

means for selecting, in response to said selector control signal, an output signal from the group consisting of said internal clocking signal and said inverted clocking signal.

14 ~~7.~~ (Original) The circuit of claim ~~6~~ 13, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

8-9. (Canceled)

15 ~~10.~~ (Previously Presented) The circuit of claim ~~6~~ 13, further comprising:

means for latching said DTE data signal, the means for latching being clocked by said internal clocking signal.

16 11. (Currently Amended) A method for detecting and eliminating clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

~~providing a master clock signal;~~

~~deriving a DCE clocking signal and~~ providing an internal clocking signal having the same frequency as the DCE clocking signal ~~from said master clock signal, said internal clocking signal and said DCE clocking signal having a first frequency that is a fraction of the frequency of the master clock signal~~;

obtaining a first sample of said DTE data signal at a first time and a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the time interval between said first time and said second time being less than the period of the DCE clocking signal;

comparing said first sample to said second sample; ~~and~~

determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time, a transition being determined when said first sample is not equal to said second sample, wherein the transition is indicative of a clocking error; and

eliminating a detected clocking error by inverting either one of the DCE clocking signal or internal clocking signal.

17 12. (Original) The method of claim 16 11, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

18 13. (Original) The method of claim 16 11, further comprising the step of:

generating a selector control signal if said first sample is different from said second sample.

20 ~~14.~~ (Previously Presented) The method of claim ~~13~~ 18, further comprising the steps of:

inverting said DCE clocking signal to produce an inverted clocking signal; and

producing said internal clocking signal that is selected, in response to said selector control signal, from the group consisting of said DCE clocking signal and said inverted clocking signal.

21 ~~15.~~ (Previously Presented) The method of claim ~~14~~ 20, further comprising the step of:

latching said DTE data signal.

6 ~~16.~~ (Previously Presented) The circuit of claim ~~5~~, further comprising:

a data latch, clocked by said internal clocking signal, for latching said DTE data signal.

17-18. (Canceled)

7 ~~19.~~ (Previously Presented) The circuit of claim ~~16~~ 6, wherein said first enable signal is generated on the rising edge of said output signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

8 ~~20.~~ (Previously Presented) The circuit of claim ~~16~~ 6, wherein said first enable signal is generated one master clock period before the rising edge of said internal clocking signal and said second enable signal is generated one master clock period after the rising edge of said internal clocking signal.

21-24. (Canceled)

22 25. (Previously Presented) The method of claim ~~15~~ 21, further comprising the step of:

performing said obtaining step and said latching step according to a time sequence referenced to said internal clocking signal.

26. (Canceled)

9 27. (Previously Presented) The circuit of claim 4, wherein the clock generating circuit comprises:

a clock generator that generates said internal clocking signal;

an inverter that produces an inverted clocking signal from the internal clocking signal; and

a selector that receives the internal clocking signal and the inverted clocking signal and produces the DCE clocking signal that is selected, in response to the selector control signal, from the group consisting of the internal clocking signal and the inverted clocking signal.

10 28. (Previously Presented) The circuit of claim ~~27~~ 9, further comprising:

a data latch, clocked by said internal clocking signal, for latching said DTE data signal.

19 29. (Previously Presented) The method of claim ~~13~~ 18, further comprising the steps of:

inverting said internal clocking signal to produce an inverted clocking signal; and

producing said DCE clocking signal that is selected, in response to said selector control signal, from the group consisting of said internal clocking signal and said inverted clocking signal.

11 30. (New) The circuit of claim 10 28, wherein said first enable signal is generated on the rising edge of said internal clocking signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

12 31. (New) The circuit of claim 10 28, wherein said first enable signal is generated one master clock period before the rising edge of said internal clocking signal and said second enable signal is generated one master clock period after the rising edge of said internal clocking signal.